# SECTION 3
# OVERVIEW

This section contains information about the entire MC68336/376 modular microcontroller. It lists the features of each module, shows device functional divisions and pin assignments, summarizes signal and pin functions, discusses the intermodule bus, and provides system memory maps. Timing and electrical specifications for the entire microcontroller and for individual modules are provided in **APPENDIX A ELECTRICAL CHARACTERISTICS**. Comprehensive module register descriptions and memory maps are provided in **APPENDIX D REGISTER SUMMARY**.

## 3.1 MCU Features

The following paragraphs highlight capabilities of each of the microcontroller modules. Each module is discussed separately in a subsequent section of this user's manual.

### 3.1.1 Central Processing Unit (CPU32)

- 32-bit architecture
- Virtual memory implementation
- Table look-up and interpolate instruction
- Improved exception handling for controller applications
- High level language support
- Background debug mode
- Fully static operation

### 3.1.2 System Integration Module (SIM)

- External bus support
- Programmable chip select outputs
- System protection logic
- Watchdog timer, clock monitor and bus monitor
- Two 8-bit dual function input/output ports
- One 7-bit dual function output port
- Phase-locked loop (PLL) clock system

### 3.1.3 Standby RAM Module (SRAM)

- 4-Kbytes of static RAM
- No standby supply

### 3.1.4 Masked ROM Module (MRM)

- 8-Kbyte array, accessible as bytes or words
- User selectable default base address
- User selectable bootstrap ROM function
- User selectable ROM verification code

### 3.1.5 10-Bit Queued Analog-to-Digital Converter (QADC)

- 16 channels internally; up to 44 directly accessible channels with external multiplexing
- Six automatic channel selection and conversion modes
- Two channel scan queues of variable length, each with a variable number of subqueues
- 40 result registers and three result alignment formats
- Programmable input sample time
- Direct control of external multiplexers

### 3.1.6 Queued Serial Module (QSM)

- Enhanced serial communications interface (SCI)
- Modulus baud rate generator
- Parity detection
- Queued serial peripheral interface (QSPI)
- 80-byte static RAM to perform queued operations
- Up to 16 automatic transfers
- Continuous cycling, 8 to 16 bits per transfer, LSB or MSB first
- Dual function I/O pins

### 3.1.7 Configurable Timer Module Version 4 (CTM4)

- Two 16-bit modulus counter submodules (MCSMs)
- 16-bit free-running counter submodule (FCSM)
- Four double-action submodules (DASMs)
- Four pulse-width submodules (PWMSMs)

### 3.1.8 Time Processor Unit (TPU)

- Dedicated micro-engine operating independently of the CPU32
- 16 independent programmable channels and pins
- Each channel has an event register consisting of a 16-bit capture register, a 16-bit compare register and a 16-bit comparator
- Any channel can perform any time function
- Each channel has six or eight 16-bit parameter registers
- Each timer function may be assigned to more than one channel
- Two timer counter registers with programmable prescalers
- Each channel can be synchronized to one or both counters
- Selectable channel priority levels

### 3.1.9 Static RAM Module with TPU Emulation Capability (TPURAM)

- 3.5 Kbytes of static RAM
- External VSTBY pin for separate standby supply
- May be used as normal RAM or TPU microcode emulation RAM

### 3.1.10 CAN 2.0B Controller Module (TouCAN)

- Full implementation of CAN protocol specification, version 2.0 A and B
- 16 receive/transmit message buffers of 0 to 8 bytes data length
- Global mask register for message buffers 0 to 13
- Independent mask registers for message buffers 14 and 15
- Programmable transmit-first scheme: lowest ID or lowest buffer number
- 16-bit free-running timer for message time-stamping
- Low power sleep mode with programmable wake-up on bus activity

## 3.2 Intermodule Bus

The intermodule bus (IMB) is a standardized bus developed to facilitate both design and operation of modular microcontrollers. It contains circuitry to support exception processing, address space partitioning, multiple interrupt levels, and vectored interrupts. The standardized modules in the MCU communicate with one another through the IMB. The IMB in the MCU uses 24 address and 16 data lines.

## 3.3 System Block Diagram and Pin Assignment Diagrams

**Figure 3-1** is a functional diagram of the MCU. There is not a one-to-one correspondence between location and size of blocks in the diagram and location and size of integrated-circuit modules. **Figure 3-2** shows the MC68336 pin assignment package; **Figure 3-3** shows the MC68376 pin assignment package. Note that the MC68376 is a pin-compatible upgrade for the MC68336 that provides a CAN protocol controller and an 8-Kbyte masked ROM module. Both devices use a 160-pin plastic surface-mount package. Refer to **B.1 Obtaining Updated MC68336/376 Mechanical Information** for package dimensions. Refer to subsequent paragraphs in this section for pin and signal descriptions.

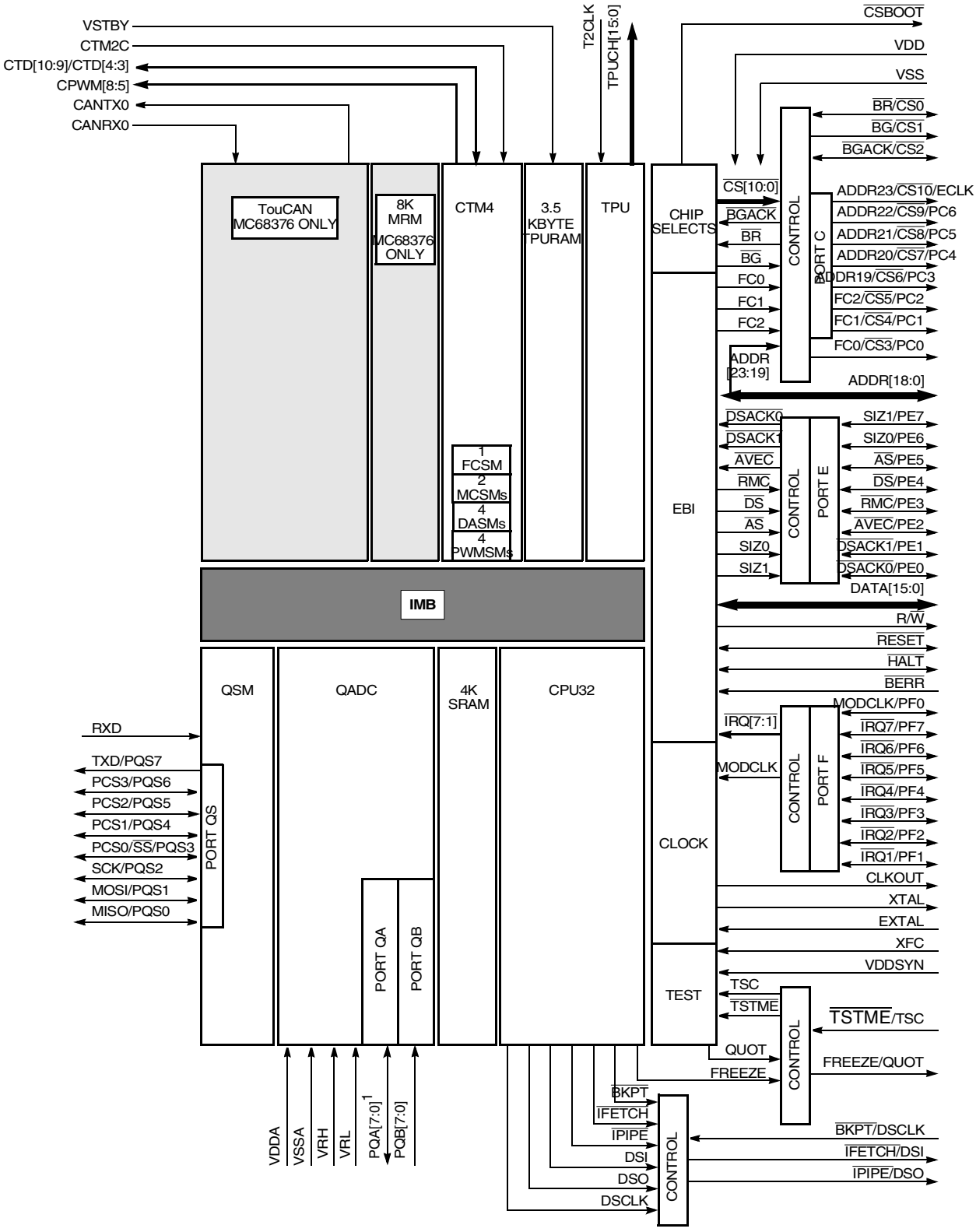
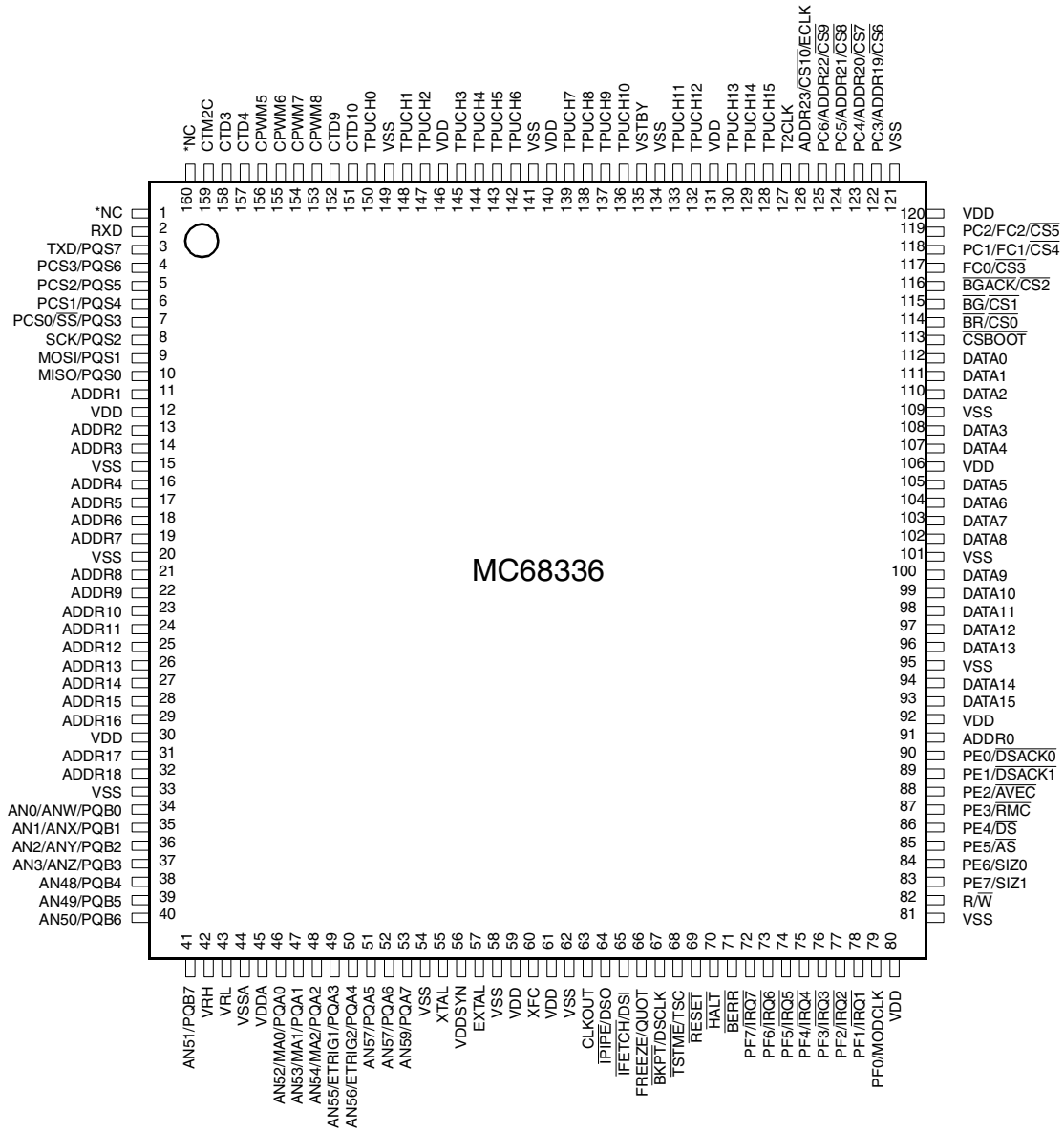



**Figure 3-1 MC68336/376 Block Diagram**




*NOTE: MC68336 REVISION D AND LATER (F60K AND LATER MASK SETS) HAVE ASSIGNED PINS 1 AND 160 AS “NO CONNECT”, TO ALLOW PIN COMPATIBILITY WITH THE MC68376. FOR REVISION C (D65J MASK SET) DEVICES, PIN 1 IS $V_{SS}$ AND PIN 160 IS $V_{DD}$.

**Figure 3-2 MC68336 Pin Assignments for 160-Pin Package**

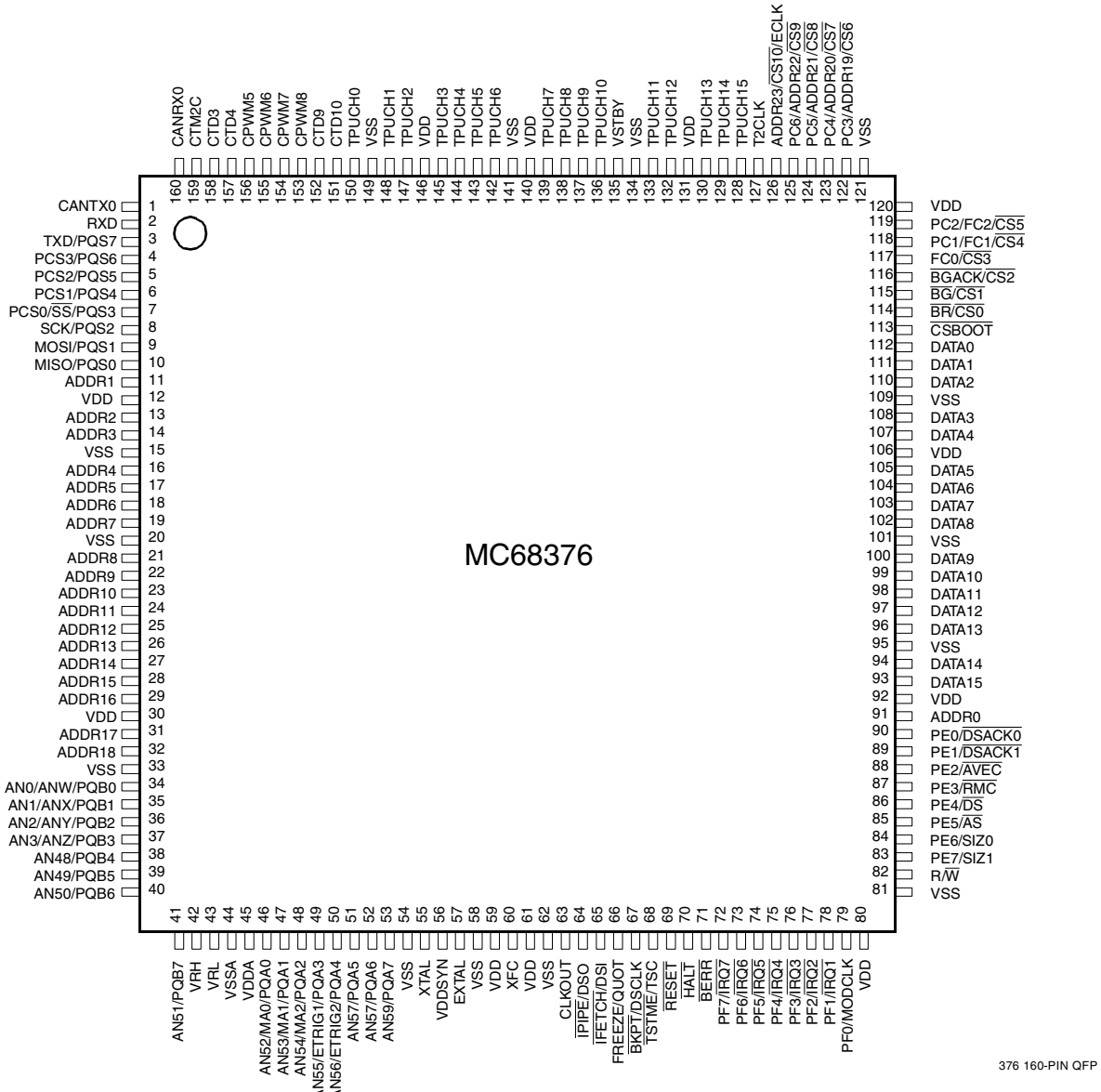



**Figure 3-3 MC68376 Pin Assignments for 160-Pin Package**

## 3.4 Pin Descriptions

The following tables summarize the functional characteristics of MC68336/376 pins. **Table 3-1** shows all inputs and outputs. Digital inputs and outputs use CMOS logic levels. An entry in the “Discrete I/O” column indicates that a pin can also be used for general-purpose input, output, or both. The I/O port designation is given when it applies. Refer to **Figure 3-1** for port organization. **Table 3-2** shows types of output drivers. **Table 3-3** shows the characteristics of power pins.

## Table 3-1 MC68336/376 Pin Characteristics

| Pin Mnemonic | Output Driver | Input Synchronized | Input Hysteresis | Discrete I/O | Port Designation |
|---|---|---|---|---|---|
| ADDR23/$\overline{CS10}$/ECLK | A | Yes | No | O | — |
| ADDR[22:19]/$\overline{CS[9:6]}$ | A | Yes | No | O | PC[6:3] |
| ADDR[18:0] | A | Yes | No | — | — |
| AN[51:48] | — | Yes[1] | Yes | I | PQB[7:4] |
| AN[3:0]/AN[w, x, y, z] | — | Yes[1] | Yes | I | PQB[3:0] |
| AN[59:57] | Ba | Yes | Yes | I/O | PQA[7:5] |
| AN[56:55]/ETRIG[2:1] | Ba | Yes | Yes | I/O | PQA[4:3] |
| AN[54:52]/MA[2:0] | Ba | Yes | Yes | I/O | PQA[2:0] |
| $\overline{AS}$ | B | Yes | Yes | I/O | PE5 |
| $\overline{AVEC}$ | B | Yes | No | I/O | PE2 |
| $\overline{BERR}$ | B | Yes | No | — | — |
| $\overline{BG}$/$\overline{CS1}$ | B | — | — | — | — |
| $\overline{BGACK}$/$\overline{CS2}$ | B | Yes | No | — | — |
| $\overline{BKPT}$/DSCLK | — | Yes | Yes | — | — |
| $\overline{BR}$/$\overline{CS0}$ | B | Yes | No | O | — |
| CLKOUT | A | — | — | — | — |
| CANRX0 (MC68376 Only) | — | Yes | Yes | — | — |
| CANTX0 (MC68376 Only) | Bo | — | — | — | — |
| $\overline{CSBOOT}$ | B | — | — | — | — |
| CTD[10:9]/[4:3] | A | Yes | Yes | I/O | — |
| CPWM[8:5] | A | — | — | O | — |
| CTM2C | — | Yes | Yes | I | — |
| DATA[15:0] | Aw | Yes[1] | No | — | — |
| $\overline{DS}$ | B | Yes | Yes | I/O | PE4 |
| $\overline{DSACK[1:0]}$ | B | Yes | No | I/O | PE[1:0] |
| EXTAL[2] | — | — | Special | — | — |
| FC[2:0]/$\overline{CS[5:3]}$ | A | Yes | No | O | PC[2:0] |
| FREEZE/QUOT | A | — | — | — | — |
| $\overline{IPIPE}$/DSO | A | — | — | O | — |
| $\overline{IFETCH}$/DSI | A | Yes | Yes | — | — |
| $\overline{HALT}$ | Bo | Yes | No | — | — |
| $\overline{IRQ[7:1]}$ | B | Yes | Yes | I/O | PF[7:1] |
| MISO | Bo | Yes[1] | Yes | I/O | PQS0 |
| MODCLK | B | Yes[1] | Yes | I/O | PF0 |
| MOSI | Bo | Yes[1] | Yes | I/O | PQS1 |
| PCS0/$\overline{SS}$ | Bo | Yes[1] | Yes | I/O | PQS3 |
| PCS[3:1] | Bo | Yes[1] | Yes | I/O | PQS[6:4] |
| R/$\overline{W}$ | A | Yes | No | — | — |

### Table 3-1 MC68336/376 Pin Characteristics (Continued)

| Pin Mnemonic | Output Driver | Input Synchronized | Input Hysteresis | Discrete I/O | Port Designation |
|---|---|---|---|---|---|
| $\overline{\text{RESET}}$ | Bo | Yes | Yes | — | — |
| $\overline{\text{RMC}}$ | B | Yes | Yes | I/O | PE3 |
| RXD | — | No | Yes | — | — |
| SCK | Bo | Yes[1] | Yes | I/O | PQS2 |
| SIZ[1:0] | B | Yes | Yes | I/O | PE[7:6] |
| T2CLK | — | Yes | Yes | — | — |
| TPUCH[15:0] | A | Yes | Yes | — | — |
| $\overline{\text{TSTME}}$/TSC | — | Yes | Yes | — | — |
| TXD | Bo | Yes[1] | Yes | I/O | PQS7 |
| XFC[2] | — | — | — | Special | — |
| XTAL[2] | — | — | — | Special | — |

NOTES:
1. DATA[15:0] are synchronized during reset only. MODCLK, and the QSM and QADC pins are synchronized only when used as input port pins.
2. EXTAL, XFC and XTAL are clock reference connections.

### Table 3-2 MC68336/376 Output Driver Types

| Type | Description |
|---|---|
| A | Output only signals that are always driven. No external pull-up required. |
| Ao | Type A output that can be operated in an open-drain mode. |
| Aw | Type A output with p-channel precharge when reset. |
| B | Three-state output that includes circuitry to assert output before high impedance is established, to ensure rapid rise time. An external holding resistor is required to maintain logic level while in the high-impedance state. |
| Bo | Type B output that can be operated in an open-drain mode. |
| Ba | Three-state output that can be operated in open-drain mode only. |

### Table 3-3 MC68336/376 Power Connections

| Pin | Description |
|---|---|
| $V_{STBY}$ | Standby RAM power |
| $V_{DDSYN}$ | Clock synthesizer power |
| $V_{DDA}$, $V_{SSA}$ | QADC converter power |
| $V_{RH}$, $V_{RL}$ | QADC reference voltage |
| $V_{SS}$, $V_{DD}$ | Microcontroller power |

## 3.5 Signal Descriptions

The following tables define the MC68336/376 signals. **Table 3-4** shows signal origin, type, and active state. **Table 3-5** describes signal functions. Both tables are sorted alphabetically by mnemonic. MCU pins often have multiple functions. More than one description can apply to a pin.

## Table 3-4 MC68336/376 Signal Characteristics

| Signal Name | MCU Module | Signal Type | Active State |
|---|---|---|---|
| ADDR[23:0] | SIM | Bus | — |
| AN[59:48]/[3:0] | QADC | Input | — |
| AN[w, x, y, z] | QADC | Input | — |
| $\overline{AS}$ | SIM | Output | 0 |
| $\overline{AVEC}$ | SIM | Input | 0 |
| $\overline{BERR}$ | SIM | Input | 0 |
| $\overline{BG}$ | SIM | Output | 0 |
| $\overline{BGACK}$ | SIM | Input | 0 |
| $\overline{BKPT}$ | CPU32 | Input | 0 |
| $\overline{BR}$ | SIM | Input | 0 |
| CLKOUT | SIM | Output | — |
| CANRX0 (MC68376 Only) | TouCAN | Input | — |
| CANTX0 (MC68376 Only) | TouCAN | Output | — |
| $\overline{CS[10:0]}$ | SIM | Output | 0 |
| $\overline{CSBOOT}$ | SIM | Output | 0 |
| CPWM[8:5] | CTM4 | Output | — |
| CTD[10:9]/[4:3] | CTM4 | Input/Output | — |
| CTM2C | CTM4 | Input | — |
| DATA[15:0] | SIM | Bus | — |
| DS | SIM | Output | 0 |
| $\overline{DSACK[1:0]}$ | SIM | Input | 0 |
| DSCLK | CPU32 | Input | Serial Clock |
| DSI | CPU32 | Input | Serial Data |
| DSO | CPU32 | Output | Serial Data |
| ECLK | SIM | Output | — |
| ETRIG[2:1] | QADC | Input | — |
| EXTAL | SIM | Input | — |
| FC[2:0] | SIM | Output | — |
| FREEZE | SIM | Output | 1 |
| $\overline{HALT}$ | SIM | Input/Output | 0 |
| $\overline{IFETCH}$ | CPU32 | Output | 0 |
| $\overline{IPIPE}$ | CPU32 | Output | 0 |
| $\overline{IRQ[7:1]}$ | SIM | Input | 0 |
| MA[2:0] | QADC | Output | 1 |
| MISO | QSM | Input/Output | — |
| MODCLK | SIM | Input | — |
| MOSI | QSM | Input/Output | — |
| PC[6:0] | SIM | Output | — |
| PCS[3:0] | QSM | Input/Output | — |
| PE[7:0] | SIM | Input/Output | — |
| PF[7:0] | SIM | Input/Output | — |

**Table 3-4 MC68336/376 Signal Characteristics (Continued)**

| Signal Name | MCU Module | Signal Type | Active State |
|---|---|---|---|
| PQA[7:0] | QADC | Input/Output | — |
| PQB[7:0] | QADC | Input | — |
| PQS[7:0] | QSM | Input/Output | — |
| QUOT | SIM | Output | — |
| R/$\overline{W}$ | SIM | Output | 1/0 |
| $\overline{RESET}$ | SIM | Input/Output | 0 |
| $\overline{RMC}$ | SIM | Output | 0 |
| RXD | QSM | Input | — |
| SCK | QSM | Input/Output | — |
| SIZ[1:0] | SIM | Output | 1 |
| $\overline{SS}$ | QSM | Input | 0 |
| T2CLK | TPU | Input | — |
| TPUCH[15:0] | TPU | Input/Output | — |
| $\overline{TSTME}$/TSC | SIM | Input | 0/1 |
| TXD | QSM | Output | — |
| XFC | SIM | Input | — |
| XTAL | SIM | Output | — |

## Table 3-5 MC68336/376 Signal Functions

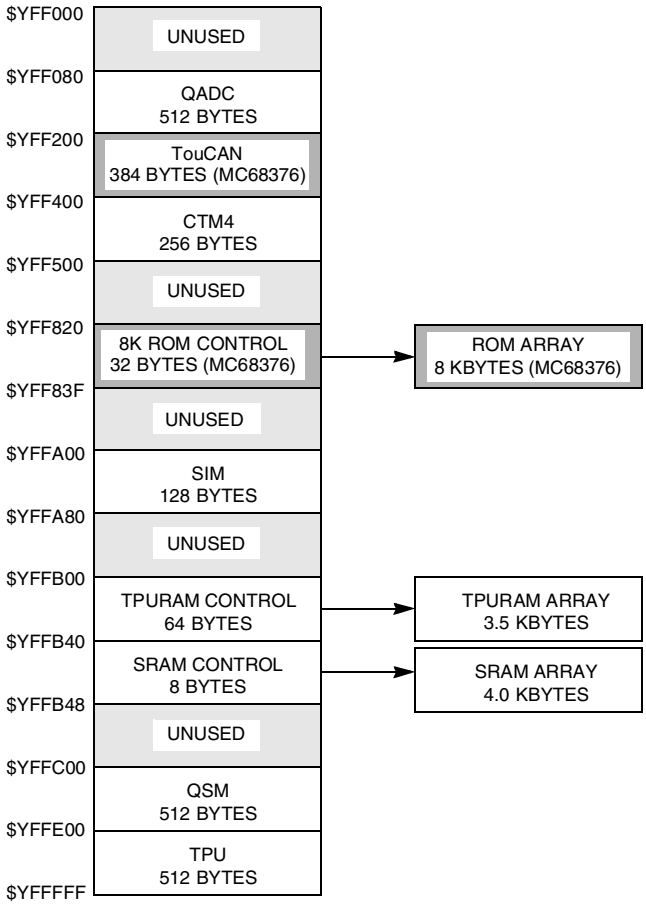
| Mnemonic | Signal Name | Function |
|---|---|---|
| ADDR[23:0] | Address Bus | 24-bit address bus used by the CPU32 |
| AN[59:48]/[3:0] | QADC Analog Input | 16 channel A/D converter analog input pins |
| AN[w, x, y, z] | QADC Analog Input | Four input channels utilized when operating in multiplexed mode |
| $\overline{\text{AS}}$ | Address Strobe | Indicates that a valid address is on the address bus |
| $\overline{\text{AVEC}}$ | Autovector | Requests an automatic vector during interrupt acknowledge |
| $\overline{\text{BERR}}$ | Bus Error | Indicates that a bus error has occurred |
| $\overline{\text{BG}}$ | Bus Grant | Indicates that the MCU has relinquished the bus |
| $\overline{\text{BGACK}}$ | Bus Grant Acknowledge | Indicates that an external device has assumed bus mastership |
| $\overline{\text{BKPT}}$ | Breakpoint | Signals a hardware breakpoint to the CPU |
| $\overline{\text{BR}}$ | Bus Request | Indicates that an external device requires bus mastership |
| CLKOUT | System Clock Out | System clock output |
| CANRX0 | TouCAN Receive Data | CAN serial data input |
| CANTX0 | TouCAN Transmit Data | CAN serial data output |
| $\overline{\text{CS}}$[10:0] | Chip-Selects | Select external devices at programmed addresses |
| $\overline{\text{CSBOOT}}$ | Boot Chip-Select | Chip-select for external bootstrap memory |
| CPWM[8:5] | CTM4 PWMs | Four pulse-width modulation channels |
| CTD[10:9]/[4:3] | CTM4 Double Action Channels | Bidirectional double action timer channels |
| CTM2C | CTM4 Modulus Clock | Modulus counter clock input |
| DATA[15:0] | Data Bus | 16-bit data bus used by the CPU32 |
| $\overline{\text{DS}}$ | Data Strobe | Indicates that an external device should place valid data on the data bus during a read cycle and that valid data has been placed on the data bus by the CPU during a write cycle. |
| $\overline{\text{DSACK}}$[1:0] | Data and Size Acknowledge | Provides asynchronous data transfers and dynamic bus sizing |
| DSI, DSO, DSCLK | Developmental Serial In, Out, Clock | Serial I/O and clock for background debug mode |
| ECLK | E-Clock | M6800 bus clock output |
| ETRIG[2:1] | QADC External Trigger | External trigger pins used when a QADC scan queue is in external trigger mode |
| EXTAL, XTAL | Crystal Oscillator | Connections for clock synthesizer circuit reference; a crystal or an external oscillator can be used |
| FC[2:0] | Function Codes | Identify processor state and current address space |
| FREEZE | Freeze | Indicates that the CPU has acknowledged a breakpoint |
| $\overline{\text{HALT}}$ | Halt | Suspend external bus activity |
| $\overline{\text{IFETCH}}$ | Instruction Pipeline | Indicates instruction pipeline activity |
| $\overline{\text{IPIPE}}$ | Instruction Pipeline | Indicates instruction pipeline activity |
| $\overline{\text{IRQ}}$[7:1] | Interrupt Request | Requests an interrupt of specified priority level from the CPU |
| MA[2:0] | QADC Multiplexed Address | When external multiplexing is used, these pins provide addresses to the external multiplexer |
| MISO | Master In, Slave Out | Serial input to QSPI in the master mode; serial output from QSPI in the slave mode |
| MODCLK | Clock Mode Select | Selects the source of the system clock |

**Table 3-5 MC68336/376 Signal Functions (Continued)**

| Mnemonic | Signal Name | Function |
|---|---|---|
| MOSI | Master Out, Slave In | Serial output from the QSPI in master mode; serial input to the QSPI in slave mode |
| PC[6:0] | Port C | SIM digital output port signals |
| PCS[3:0] | Peripheral Chip-Selects | QSPI peripheral chip-select |
| PE[7:0] | Port E | SIM digital input/output port signals |
| PF[7:0] | Port F | SIM digital input/output port signals |
| PQA[7:0] | QADC Port A | QADC port A digital input/output port signals |
| PQB[7:0] | QADC Port B | QADC port B digital input port signals |
| PQS[7:0] | Port QS | QSM digital input/output port signals |
| QUOT | Quotient Out | Provides the quotient bit of the polynomial divider (test mode only) |
| R/$\overline{W}$ | Read/Write | Indicates the direction of data transfer on the bus |
| $\overline{RESET}$ | Reset | System reset |
| $\overline{RMC}$ | Read-Modify-Write Cycle | Indicates an indivisible read-modify-write instruction |
| RXD | SCI Receive Data | Serial input to the SCI |
| SCK | QSPI Serial Clock | Clock output from QSPI in master mode; clock input to QSPI in slave mode |
| SIZ[1:0] | Size | Indicates the number of bytes remaining to be transferred during a bus cycle |
| $\overline{SS}$ | Slave Select | Starts serial transmission when QSPI is in slave mode; chip-select in master mode |
| T2CLK | TPU Clock | TPU clock input |
| TPUCH[15:0] | TPU I/O Channels | Bidirectional TPU channels |
| TSC | Three-State Control | Places all output drivers in a high impedance state |
| $\overline{TSTME}$ | Test Mode Enable | Hardware enable for SIM test mode |
| TXD | SCI Transmit Data | Serial output from the SCI |
| XFC | External Filter Capacitor | Connection for external phase-locked loop filter capacitor |

## 3.6 Internal Register Map

In **Figure 3-4**, IMB ADDR[23:20] are represented by the letter Y. The value represented by Y determines the base address of MCU module control registers. In the MC68336/376, Y is equal to M111, where M is the logic state of the module mapping (MM) bit in the system integration module configuration register (SIMCR).




NOTES: 1. Y=M111, WHERE M IS THE MODMAP SIGNAL STATE ON THE IMB, WHICH REFLECTS THE STATE OF THE MODMAP IN THE MODULE CONFIGURATION REGISTER OF THE SYSTEM INTEGRATION MODULE. (Y=$7 OR $F)

2. ATTEMPTED ACCESSES TO UNUSED LOCATIONS OR UNUSED BITS WITHIN VALID LOCATIONS RETURN ALL ZEROS.

336/376 ADDRESS MAP

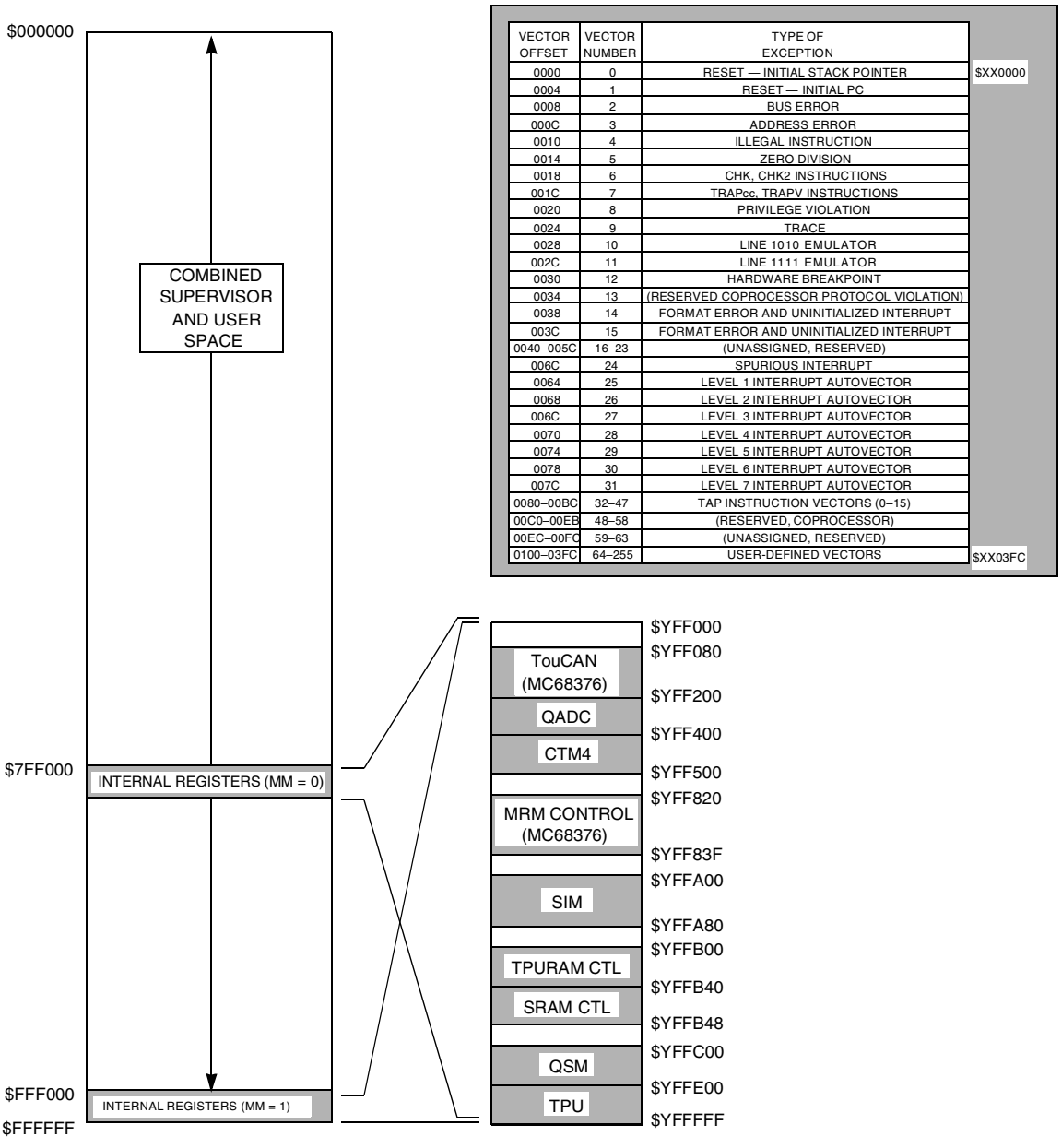
**Figure 3-4 MC68336/376 Address Map**

## 3.7 Address Space Maps

Figure 3-5 shows a single memory space. Function codes FC[2:0] are not decoded externally so that separate user/supervisor or program/data spaces are not provided. In Figure 3-6, FC2 is decoded, resulting in separate supervisor and user spaces. FC[1:0] are not decoded, so that separate program and data spaces are not provided. In **Figures** 3-7 and 3-8, FC[2:0] are decoded, resulting in four separate memory spaces: supervisor/program, supervisor/data, user/program and user/data.

All exception vectors are located in supervisor data space, except the reset vector, which is located in supervisor program space. Only the initial reset vector is fixed in the processor's memory map. Once initialization is complete, there are no fixed assignments. Since the vector base register (VBR) provides the base address of the

vector table, the vector table can be located anywhere in memory. Refer to **SECTION 4 CENTRAL PROCESSOR UNIT** for more information concerning memory management, extended addressing, and exception processing. Refer to **5.5.1.7 Function Codes** for more information concerning function codes and address space types.

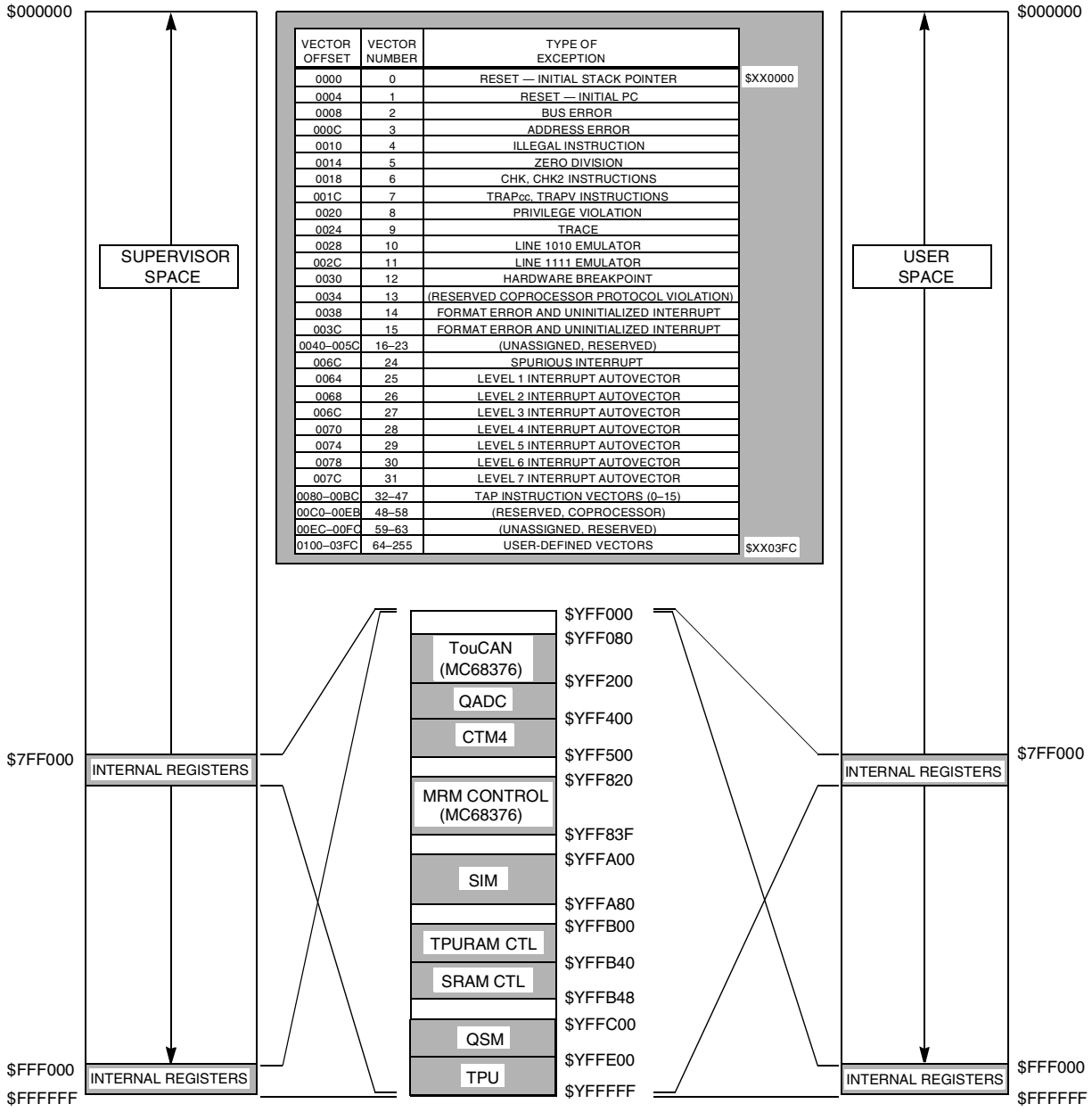



| VECTOR OFFSET | VECTOR NUMBER | TYPE OF EXCEPTION | |
|---|---|---|---|
| 0000 | 0 | RESET — INITIAL STACK POINTER | $XX0000 |
| 0004 | 1 | RESET — INITIAL PC | |
| 0008 | 2 | BUS ERROR | |
| 000C | 3 | ADDRESS ERROR | |
| 0010 | 4 | ILLEGAL INSTRUCTION | |
| 0014 | 5 | ZERO DIVISION | |
| 0018 | 6 | CHK, CHK2 INSTRUCTIONS | |
| 001C | 7 | TRAPcc, TRAPV INSTRUCTIONS | |
| 0020 | 8 | PRIVILEGE VIOLATION | |
| 0024 | 9 | TRACE | |
| 0028 | 10 | LINE 1010 EMULATOR | |
| 002C | 11 | LINE 1111 EMULATOR | |
| 0030 | 12 | HARDWARE BREAKPOINT | |
| 0034 | 13 | (RESERVED COPROCESSOR PROTOCOL VIOLATION) | |
| 0038 | 14 | FORMAT ERROR AND UNINITIALIZED INTERRUPT | |
| 003C | 15 | FORMAT ERROR AND UNINITIALIZED INTERRUPT | |
| 0040–005C | 16–23 | (UNASSIGNED, RESERVED) | |
| 006C | 24 | SPURIOUS INTERRUPT | |
| 0064 | 25 | LEVEL 1 INTERRUPT AUTOVECTOR | |
| 0068 | 26 | LEVEL 2 INTERRUPT AUTOVECTOR | |
| 006C | 27 | LEVEL 3 INTERRUPT AUTOVECTOR | |
| 0070 | 28 | LEVEL 4 INTERRUPT AUTOVECTOR | |
| 0074 | 29 | LEVEL 5 INTERRUPT AUTOVECTOR | |
| 0078 | 30 | LEVEL 6 INTERRUPT AUTOVECTOR | |
| 007C | 31 | LEVEL 7 INTERRUPT AUTOVECTOR | |
| 0080–00BC | 32–47 | TAP INSTRUCTION VECTORS (0–15) | |
| 00C0–00EB | 48–58 | (RESERVED, COPROCESSOR) | |
| 00EC–00FC | 59–63 | (UNASSIGNED, RESERVED) | |
| 0100–03FC | 64–255 | USER-DEFINED VECTORS | $XX03FC |

NOTES:
1. LOCATION OF THE EXCEPTION VECTOR TABLE IS DETERMINED BY THE VECTOR BASE REGISTER. THE VECTOR ADDRESS IS THE CONCATENATION OF THE UPPER 22 BITS OF THE VBR WITH THE 8-BIT VECTOR NUMBER OF THE INTERRUPTING MODULE. THE RESULT IS LEFT JUSTIFIED TO FORCE LONG WORD ALIGNMENT.
2. LOCATION OF THE MODULE CONTROL REGISTERS IS DETERMINED BY THE STATE OF THE MODULE MAPPING (MM) BIT IN THE SIM CONFIGURATION REGISTER. Y = M111 WHERE M IS THE STATE OF THE MM BIT.
3. SOME UNUSED ADDRESSES WITHIN THE INTERNAL REGISTER BLOCK ARE MAPPED EXTERNALLY. REFER TO THE APPROPRIATE MODULE REFERENCE MANUAL FOR INFORMATION ON MAPPING OF UNUSED ADDRESSES WITHIN INTERNAL REGISTER BLOCKS.

336//376 S/U COMB MAP

**Figure 3-5 Overall Memory Map**

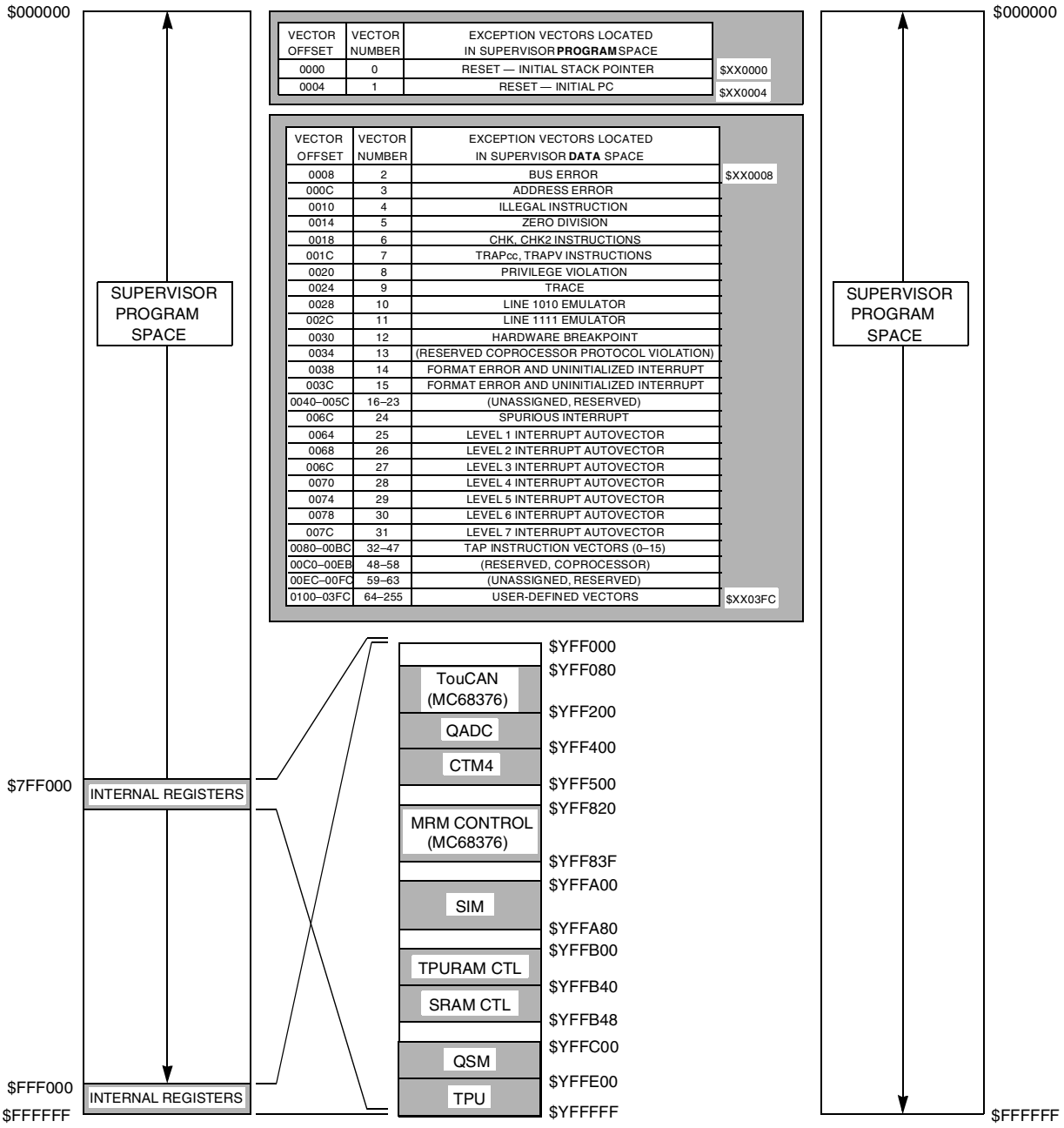



NOTES:

1. LOCATION OF THE EXCEPTION VECTOR TABLE IS DETERMINED BY THE VECTOR BASE REGISTER. THE VECTOR ADDRESS IS THE CONCATENATION OFTHE UPPER 22 BITS OF THE VBR WITH THE 8-BIT VECTOR NUMBER OF THE INTERRUPTING MODULE. THE RESULT IS LEFT JUSTIFIED TO FORCE LONG WORD ALIGNMENT.
2. LOCATION OF THE MODULE CONTROL REGISTERS IS DETERMINED BY THE STATE OF THE MODULE MAPPING (MM) BIT IN THE SIM CONFIGURATION REGISTER. Y = M111 WHERE M IS THE STATE OF THE MM BIT.
3. SOME UNUSED ADDRESSES WITHIN THE INTERNAL REGISTER BLOCK ARE MAPPED EXTERNALLY. REFER TO THE APPROPRIATE MODULE REFERENCE MANUAL FOR INFORMATION ON MAPPING OF UNUSED ADDRESSES WITHIN INTERNAL REGISTER BLOCKS.
4. SOME INTERNAL REGISTERS ARE NOT AVAILABLE IN USER SPACE.

336/376 S/U SEP MAP

**Figure 3-6 Separate Supervisor and User Space Map**




| VECTOR OFFSET | VECTOR NUMBER | EXCEPTION VECTORS LOCATED IN SUPERVISOR **PROGRAM** SPACE | |
|---|---|---|---|
| 0000 | 0 | RESET — INITIAL STACK POINTER | $XX0000 |
| 0004 | 1 | RESET — INITIAL PC | $XX0004 |

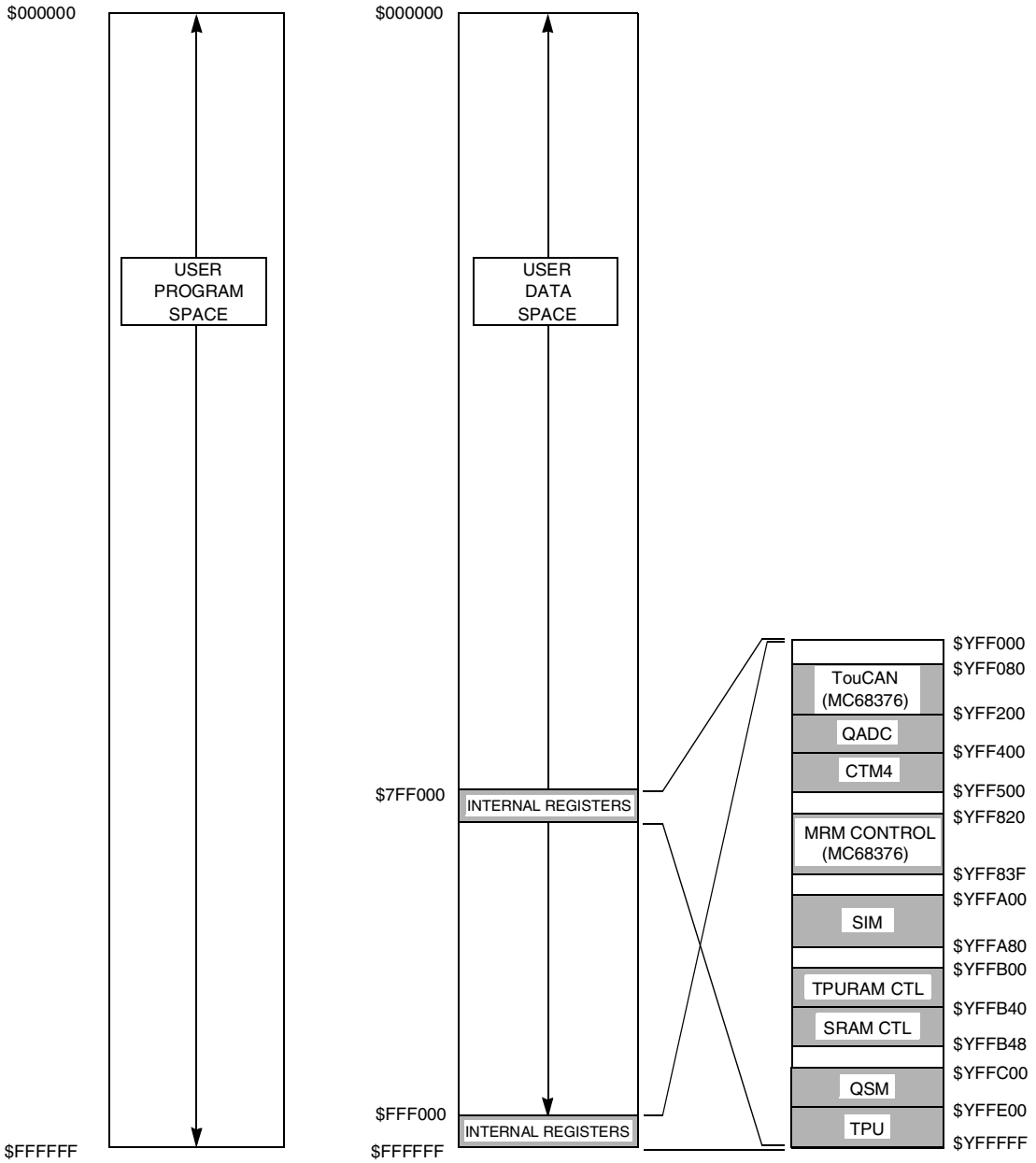
| VECTOR OFFSET | VECTOR NUMBER | EXCEPTION VECTORS LOCATED IN SUPERVISOR **DATA** SPACE | |
|---|---|---|---|
| 0008 | 2 | BUS ERROR | $XX0008 |
| 000C | 3 | ADDRESS ERROR | |
| 0010 | 4 | ILLEGAL INSTRUCTION | |
| 0014 | 5 | ZERO DIVISION | |
| 0018 | 6 | CHK, CHK2 INSTRUCTIONS | |
| 001C | 7 | TRAPcc, TRAPV INSTRUCTIONS | |
| 0020 | 8 | PRIVILEGE VIOLATION | |
| 0024 | 9 | TRACE | |
| 0028 | 10 | LINE 1010 EMULATOR | |
| 002C | 11 | LINE 1111 EMULATOR | |
| 0030 | 12 | HARDWARE BREAKPOINT | |
| 0034 | 13 | (RESERVED COPROCESSOR PROTOCOL VIOLATION) | |
| 0038 | 14 | FORMAT ERROR AND UNINITIALIZED INTERRUPT | |
| 003C | 15 | FORMAT ERROR AND UNINITIALIZED INTERRUPT | |
| 0040–005C | 16–23 | (UNASSIGNED, RESERVED) | |
| 006C | 24 | SPURIOUS INTERRUPT | |
| 0064 | 25 | LEVEL 1 INTERRUPT AUTOVECTOR | |
| 0068 | 26 | LEVEL 2 INTERRUPT AUTOVECTOR | |
| 006C | 27 | LEVEL 3 INTERRUPT AUTOVECTOR | |
| 0070 | 28 | LEVEL 4 INTERRUPT AUTOVECTOR | |
| 0074 | 29 | LEVEL 5 INTERRUPT AUTOVECTOR | |
| 0078 | 30 | LEVEL 6 INTERRUPT AUTOVECTOR | |
| 007C | 31 | LEVEL 7 INTERRUPT AUTOVECTOR | |
| 0080–00BC | 32–47 | TAP INSTRUCTION VECTORS (0–15) | |
| 00C0–00EB | 48–58 | (RESERVED, COPROCESSOR) | |
| 00EC–00FC | 59–63 | (UNASSIGNED, RESERVED) | |
| 0100–03FC | 64–255 | USER-DEFINED VECTORS | $XX03FC |

NOTES:

1. LOCATION OF THE EXCEPTION VECTOR TABLE IS DETERMINED BY THE VECTOR BASE REGISTER. THE VECTOR ADDRESS IS THE CONCATENATION OF THE UPPER 22 BITS OF THE VBR WITH THE 8-BIT VECTOR NUMBER OF THE INTERRUPTING MODULE. THE RESULT IS LEFT JUSTIFIED TO FORCE LONG WORD ALIGNMENT.
2. LOCATION OF THE MODULE CONTROL REGISTERS IS DETERMINED BY THE STATE OF THE MODULE MAPPING (MM) BIT IN THE SIM CONFIGURATION REGISTER. Y = M111 WHERE M IS THE STATE OF THE MM BIT.
3. SOME UNUSED ADDRESSES WITHIN THE INTERNAL REGISTER BLOCK ARE MAPPED EXTERNALLY. REFER TO THE APPROPRIATE MODULE REFERENCE MANUAL FOR INFORMATION ON MAPPING OF UNUSED ADDRESSES WITHIN INTERNAL REGISTER BLOCKS.
4. SOME INTERNAL REGISTERS ARE NOT AVAILABLE IN USER SPACE.

336/376 SUPER P/D MAP

**Figure 3-7 Supervisor Space (Separate Program/Data Space) Map**




NOTES:
1. LOCATION OF THE MODULE CONTROL REGISTERS IS DETERMINED BY THE STATE OF THE MODULE MAPPING (MM) BIT IN THE SIM CONFIGURATION REGISTER. Y = M111, WHERE M IS THE STATE OF THE MM BIT.
2. UNUSED ADDRESSES WITHIN THE INTERNAL REGISTER BLOCK ARE MAPPED EXTERNALLY. “RESERVED” BLOCKS ARE NOT MAPPED EXTERNALLY.
3. SOME INTERNAL REGISTERS ARE NOT AVAILABLE IN USER SPACE.

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**Figure 3-8 User Space (Separate Program/Data Space) Map**